Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 73452

B.E./B.Tech. DEGREE EXAMINATION, ARPIL/MAY 2017

Fifth Semester

Electronics and Communication Engineering

EC 2303/EC 53/10144 EC 605 — COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Sixth Semester Biomedical Engineering)

(Regulations 2008/2010)

(Also common to PTEC 2303 – Computer Architecture and Organization for B.E. (Part-Time) Fourth Semester – Electronics and Communication Engineering – Regulations 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is a register? State its role in computers.
2. Compare Instruction format with Instruction type.
3. What is a carry look ahead adder?
4. What is coprocessor and what functions are performed by the coprocessor?
5. Define superscalar processing.
6. What is meant by Nano programming?
7. What are the advantages of RISC processor?
8. What is bus arbitration?
9. List the important characteristics of RISC.
10. Explain the term handshaking related to data transfer.

PART B — (5 × 16 = 80 marks)

11. (a) Explain the various addressing modes in detail

Or

(b) (i) With suitable example explain fixed point and floating point number representation in computers. (10)

(ii) Write notes on evolution of computers. (6)

12. (a) With flow chart and numerical example explain Booth's multiplication algorithm. (16)

Or

(b) With relevant diagram and expressions, explain the operation of carry look ahead adder. (16)

13. (a) (i) Describe the organization of a typical micro programmed control unit organization with the help of a diagram. (8)

(ii) What is an instruction pipeline? Describe the organization of a four-stage pipeline with the help of diagram. (8)

Or

(b) (i) Describe the structure of a typical microprogram sequencer in detail. (8)

(ii) Describe any two techniques for dealing data dependencies in pipelined computers. (8)

14. (a) (i) Discuss in detail about the basic memory concepts. (8)

(ii) Draw and discuss the structure of the internal organization of memory. (8)

Or

(b) Why do we use cache memory? And explain the different types of mapping functions with the necessary block diagrams. (16)

15. (a) (i) Explain in detail about the bus arbitration techniques in DMA. (8)

(ii) Explain vector interrupts, PCI interrupts and pipeline interrupts in detail. (8)

Or

(b) Write short notes on

(i) RISC Processors (4)

(ii) CISC Processors (4)

(iii) Super scalar Processors (4)

(iv) Vector Processors. (4)